CMI8738

PCI-6CH C3DX series /PCI-Based HRTF 3D Extension Positional Audio Chip

DESCRIPTION

With high speed PCI V2.1 bus controller and legacy audio SBPro® DSPemulator,CMI8738 is designed for PC add-in cards and all-in-one motherboards. No external CODEC is needed in CMI8738: CMI-8738 supports the legacy audio – SBPRO™, FM emulator/DLS wavetable music synthesis, and HRTF 3D positional audio functions. Drivers support EAX®, Karaoke Key, Echo……functions. Above all CMI8738 supports PCtel® HSP56 (1789) interface.

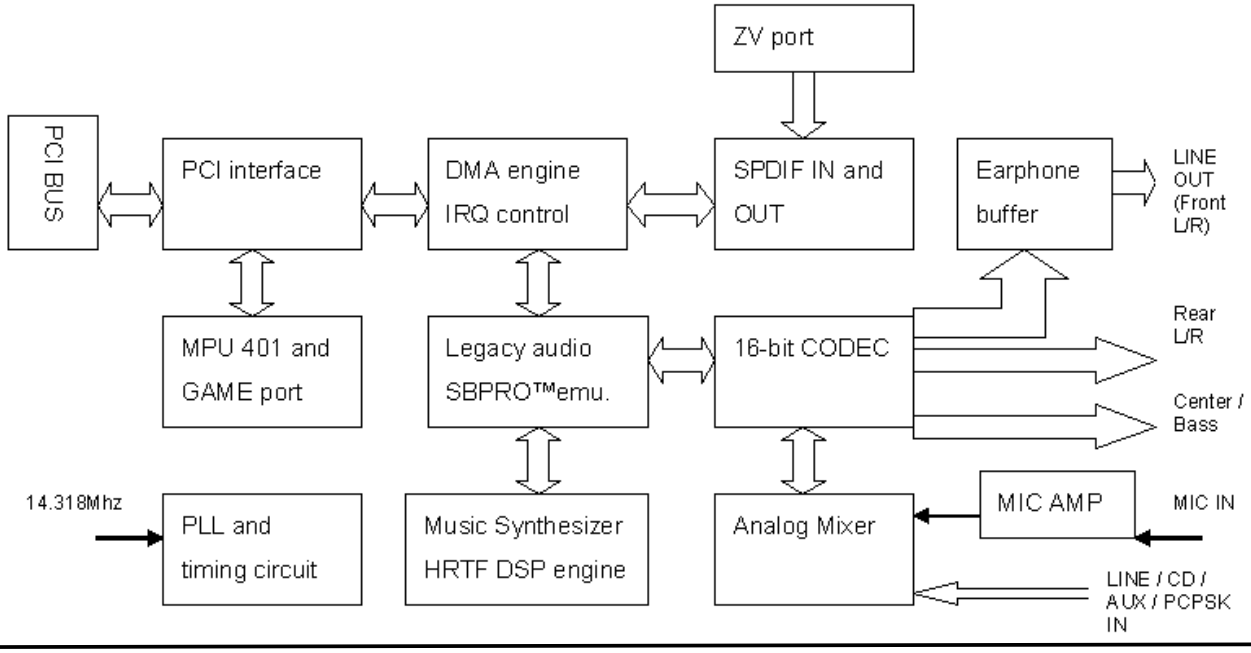
CMI8738 uses HRTF 3D extension technology to enhance traditional HRTF 3D positional audio by substituting two-speaker system by four or six - speaker one.

Being outstanding for its full audio functions, competitive price, and power management, CMI-8738 is the best choice for people seeking for optimum use of the PC applications.

FEATURES

- 6CH DAC for AC3® 5.1CH purpose.
- HRTF-based 3D positional audio, supporting DirectSound™ 3D interface
- Supports 4.1/5.1 speakers, C3DX positional audio in 4 / 6 CH speaker mode
- Legacy audio SBPRO™ compatible
- DLS-based wavetable music synthesizer, supports DirectMusic™
- Built-in 32ohm Earphone buffer
- Drivers support EAX®, Karaoke Key, Echo…
- MPU-401 port/ Dual game port
- 16-bit full duplex CODEC
- 32-bit PCI bus master
- External E²PROM interface
- Single chip design, digital power +3.3V, analog power +5V, 128 pins QFP

BLOCK DIAGRAM



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Revision History

Date	Rev.	Release Note
2010/05/03	Rev. 2.2	Format Modification

1. Description and Overview

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Being compatible with DirectSound™ 3D, CMI8738 meets PC99® requirements, and supports professional digital audio interface such as 16-bit SPDIF IN (0.5V ~ 5V)and OUT(44.1K and 48K format).

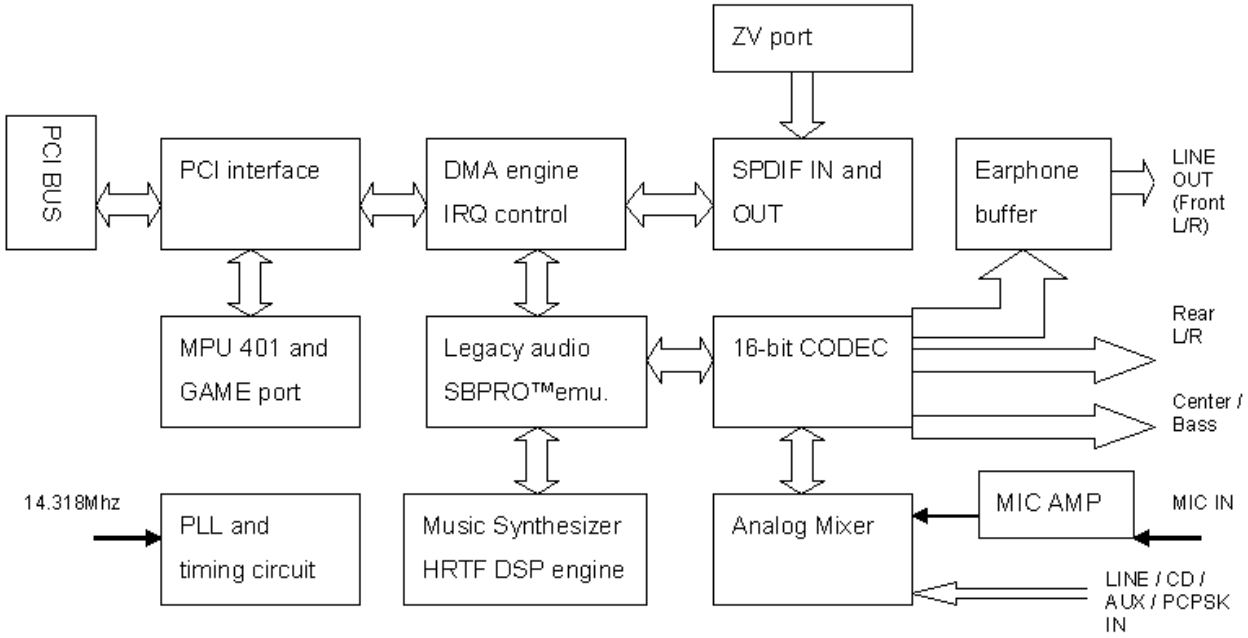
CMI8738 uses HRTF 3D extension technology to enhance traditional HRTF 3D positional audio by substituting two-speaker system by four or six - speaker one (it supports additional 2 ch 16-bit DAC to provide rear side audio and another 2 ch for subwoofer/Center). It greatly improves HRTF 3D positional audio quality and successfully removes the sweet spot limitations: users can enjoy genuine 3D audio gaming effects, and don't have to worry about the environmental confinement any more.

Being outstanding for its full audio functions, competitive price, and power management, CMI-8738 is the best choice for people seeking for optimum use of the PC applications.

2. Features

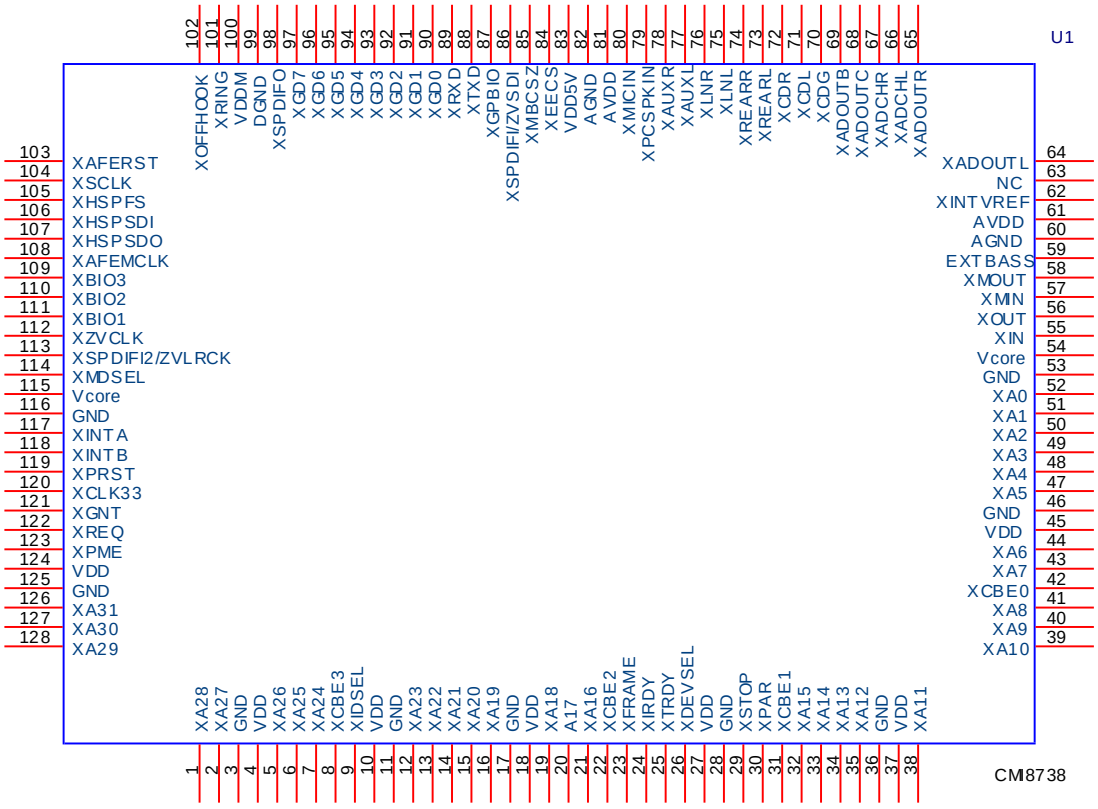
- 6CH DAC for AC3® 5.1CH purpose.
- HRTF-based 3D positional audio, supporting DirectSound™ 3D interface
- Supports 4.1/5.1 speakers, C3DX positional audio in 4 / 6 CH speaker mode
- Legacy audio SBPRO™ compatible
- DLS-based wavetable music synthesizer, supports DirectMusic™
- Professional digital audio interface supporting 24-bit SPDIF IN and OUT (44.1K and 48K format)
- Built-in 32ohm Earphone buffer
- Drivers support EAX®, Karaoke Key, Echo…
- MPU-401 port/ Dual game port
- 16-bit full duplex CODEC
- Built-in ZV port
- 32-bit PCI bus master
- External E^2PROM interface
- Single chip design, digital power +3.3V, analog power +5V, 128 pins QFP

3. Block Diagram



4. Pin Assignment

QFP 128 PINS



CMI8738/PCI-6CH C3DX AUDIO CHIP

5. Pin Description

5.1 CMI8738/PCI-6CH C3DX Series Chip Function List

Model	SPDIF/ZVport
CMI8738/PCI-6CH	YES
CMI8738/PCI-6CH-MX	YES
CMI8738/PCI-6CH-LX	NO

5.2 Digital Pin Description

Name	Number	PIN Type	Definition
XA31-XA0	126-128,1-2,5-7,12-16,19-21,32-35,38-41,43-44,47-52	I/O	PCI bus address and data lines
XINTA	117	O	Interrupt request , active-low.
XINTB	118	O	Independent Modem interrupt request (optional; unused)
XPRST	119	I	Reset
XCLK33	120	I	PCI bus clock.
XGNT	121	I	Bus master grant, active-low.
XREQ	122	O	Bus master request, tri-state output, active-low.
XPME	123	O	Power Management Event pin (optional; unused)
XIDSEL	9	I	ID select, active-high.
XFRAME	23	I/O	Cycle frame, active-low.
XIRDY	24	I/O	Initiator ready, active-low. The bus master device is ready to transmit or receive data
XTRDY	25	I/O	Target ready, active-low. The target device is ready to transmit or receive data
XDEVSEL	26	I/O	Device select, active-low. The target device has decoded the address of the current transaction as its own chip select range.
XSTOP	29	I/O	Stop transaction, active-low. The target device request to the master to stop the current transaction.
XPAR	30	I/O	Parity. The pin indicates even parity across XA31-XA9 and XCBE3-0 for both address and data phases.
XCBE3,2,1,0	8,22,31,42	I/O	Multiplexed command/byte enable. These pins indicate cycle type during the address phase of a transaction.
VDD	4,10,18,27,37,45,124	+3.3V/+5V	PCI I/O power pin
Vcore	54,115	+3.3V	Core digital circuit power pin
GND	3,11,17,28,36,46,53,116,125	GND	Digital and PCI I/O ground
XIN	55	I	14.318Mhz crystal, or external clock input
XOUT	56	O	14.318Mhz crystal
XGD7-XGD4	97-94	I	Game port switch input pin. Switch D to switch A
XGD3-XGD0	93-90	I/O	Game port resistor input pin. RC3 to RC0

Name	Number	PIN Type	Definition
XTXD	88	O	MIDI transmit data
XRXD	89	I	MIDI receive data
XSPDIFO	98	O	44.1k/48kHZ SPDIF output
XSPDIFI	86	I	44.1k/48kHZ SPDIF input
XSPDIF2	113	I	Secondary SPDIF input (5v only)
XBIO3-XBIO0	109-112	I/O	General purpose I/O
VDD5V	83	+5V	PCI I/O power pin
VDDM	100	+3.3V/+5V	PCI I/O power pin
DGND	99	GND	PCI I/O ground
XEECS	84	O	EEPROM chip select
XGPBIO	87	O	General purpose I/O pin (default=high)
XMDSEL	114	I	Modem device enable(high:enable)
XRING	101	I	Ring detection input
XOFFHOOK	102	O	Off-hook control output
XAFERST	103	O	Reset signal for MODEM DAA
XHSPFS	105	O	DAA frame SYNC
XHSPSDI	106	I	DAA data input
XHSPSDO	107	O	DAA data output
XAFEMCLK	108	O	DAA master clock
XSCLK	104	O	DAA serial clock
NC	58		
NC	57		
XMBCSZ	85	I	Audio chip select (low:enable)
ZVCLK	112	I	ZV port clock
ZVLRCK	113	I	ZV port LR channel clock
ZVSDI	86	I	ZV port data input

Remark: All PCI interface I/O pins are 3.3V signal and 5V tolerance.

5.3 Analog Pin Description

Name	Number	PIN Type	Definition
AVDD	61,81	+5V	Analog power
AGND	60,82	GND	Analog ground
XADOUTL-R	64,65	AI/O	Line out (front channels L/R)
XADCHL-R	66,67	AI/O	ADC sample hold pin
XADOUTC	68	AI/O	Center channel output
XADOUTB	69	AI/O	Bass channel output
XINTVERF	62	AO	Internal reference voltage (for testing only)
NC	63	-	Not connect
XCDL-R XCDGND	71,72,70	AI	CD audio differential input
XLNL-R	75,76	AI	Line in or Rear channels out
XAUXL-R	77,78	AI	Aux. Line in
XPCSPKIN	79	AI	PC beep signal or Mono in
XMICIN	80	AI	Microphone in
XREARL-R	73,74	AO	Rear channels L/R out
EXTBASS	59	AI	External bass channel input

5.4 Power On Configuration Pin

Name	Number	Definition
XEECS	84	4/6 channel selection. For 4 or 6 channel purpose selection. This pin tie high mean 6ch, pull down compatible with 4ch chip.

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Ratings	Symbol	Value	Units
Digital power voltage	VDD	VDD±5%	V
Analog power voltage	AVDD	AVDD±5%	V
Operating temperature range	TO	0 to 70	°C
Storage temperature range	TST	-40 to 125	°C
Maximum power dissipation	PDMAX	300	MW

6.2 Digital Characteristics

PARAMETER	Symbol	Min	Typ	Max	Unit
Input high voltage(PCI I/O)	VIH	2.		VDD+0.3	V
Input low voltage (PCI I/O)	VIL	-0.5		0.8	V
Output high voltage	VOH	2.4		VDD	V
Output low voltage	VOL	0.0	0.2	0.4	V
SPDIF IN input high voltage	VIH1		2.6		V
SPDIF IN input low voltage	VIL1		2.4		V
SPDIF output high voltage	VOH1		VDD		V
SPDIF output low voltage	VOL1		GND		V
Output low current		4	8		mA

6.3 Audio Characteristics

PARAMETER	Symbol	Min	Typ	Max	Unit
Analog input voltage	Avin		1.1		Vrms
Analog output voltage	Avout		1.1		Vrms
A-A S/N ratio			85		dB
A-A THD			0.02		%
ADC S/N ratio			72		dB
ADC THD			0.1		%
DAC S/N ratio			85		dB
DAC THD			0.05		%
SPDIF IN/OUT S/N ratio			120		dB
SPDIF IN/OUT THD			0		%
Microphone input level		20		200	mv
Microphone booster				20	dB

7. PCI Configuration Spaces (Audio)

00h 13F6 : (**Vender ID**) read only

02h 0111 : (Device ID) read only

04h 0006 : Command (State after #RST all is "**0**")

0 (bit 9) Fast back-to-back enable

0 (bit 8) #SERR enable (R/W)

0 (bit 7) Wait cycle control

0 (bit 6) Parity error response

0 (bit 5) VGA palette snoop

0 (bit 4) Memory write and invalidate enable

0 (bit 3) Special cycles

1 (bit 2) Bus master **(R/W)**

0 (bit 1) **Memory space**

1 (bit 0) I/O space **(R/W)**

06h 0280 : Status

0 (bit 15) Detected Parity Error

0 (bit 14) Signaled System Error

0 (bit 13) Received Master Abort

0 (bit 12) Received Target Abort

0 (bit 11) Signaled Target Abort

01 (bits 10-9) **DEVSEL timing** 00-fast, 01-medium, 10-slow

0 (bit 8) Data Parity Error Detected

0 (bit 7) **Fast Back-to-Back Capable**

0 (bit 6) Reserved

0 (bit 5) 0-33MHz ,1-66MHZ Capable

1 (bit 4) Capabilities List

0000 (bits 3-0) Reserved

08h 10 : Revision ID

09h 040100 : Audio device

0Ch 00 : Cache Line Size

0Dh 20 : **Latency Timer**

0Eh 00 : Header Type

0Fh 00 : BIST

10h 0000d401 : I/O of length : -65280(ffff0100h) : First Base Address register

14h 00000000 : Uninitialized : Second Base Address register

PCI Configuration Spaces

18h 00000000 : Uninitialized : Third Base Address register

1Ch 00000000 : Uninitialized : Fourth Base Address register

20h 00000000 : Uninitialized : Fifth Base Address register

24h 00000000 : Uninitialized : Sixth Base Address register

28h 00000000 : Cardbus CIS Pointer

2Ch 13f6 : (**SubSystem Vender ID**) (R/W)

2Eh 0111 : **SubSystem ID** (R/W)

30h 00000000 : Expansion ROM Base Address

34h 0000000c : Capability Pointer

38h 00000000 : Reserved

3Ch 05 : **Interrupt Line**

3Dh 01 : **Interrupt Pin**

3Eh 02 : **Min Grant**

3Fh 18 : **Max Latency**

40h 00000000: **Power management reg.**

8. PCI register

8.1 Internal Register Mapping

Function Control Register 0

Address **00**H

Bit(s)	R/W	Name	Description
31:20		Reserved.	
19		RST_CH1	Channel 1,1->Reset (Default 0)
18		RST_CH0	Channel 0,1->Reset (Default 0)
17		CHEN1	Channel 1,1->Enabled, 0->Disabled.
16		CHEN0	Channel 0,1->Enabled, 0->Disabled.
15-2		Reserved	
3		PAUSE1	Channel 1, 1->Pause if channel1 is enabled.
2		PAUSE0	Channel 0,1->Pause if channel0 is enabled.
1		CHADC1	Channel 1, 1->Recording, 0->Playback
0		CHADC0	Channel 0, 1->Recording, 0->Playback

Function Control Register 1

Address **04**H

Bit(s)	R/W	Name	Description
31-16		Reserved	
15:13		DSFC[2:0]	**Channel 1** Sampling Frequency Selection
		0 0 0	5.512 K
		0 0 1	11.025 K
		0 1 0	22.05 K
		0 1 1	44.1 K
		1 0 0	8 K
		1 0 1	16 K
		1 1 0	32 K
		1 1 1	48 K
12:10		ASFC[2:0]	**Channel 0** Sampling Frequency Selection
		0 0 0	5.512 K
		0 0 1	11.025 K
		0 1 0	22.05 K
		0 1 1	44.1 K
		1 0 0	8 K
		1 0 1	16 K
		1 1 0	32 K
		1 1 1	48 K
9		SPDF_1	SPDIF IN/OUT at Channel B at 44.1K double-words/sec.
8		SPDF_0	SPDIF OUT only at Channel A at 44.1K double-words/sec.
7		SPDFLOOP	external SPDIF/IN loopback to external SPDIF/OUT .
6		SPDO2DAC	SPDIF/OUT can be heard from internal DAC.
5		INTRM	Interrupt Mask bit for MCB (Master control block) module interrupt. 0 MCB interrupt disabled. 1 MCB interrupt enabled.
4		BREQ	If this bit is set low it will prevent the MCB and DAC/ADC block from accessing the memory. 0 Bus Master request disabled(power on state) 1 Bus Master request enabled.
3		VOICE_EN	This bit enables Legacy Voice device(SB16,FM). 0 Legacy Voice disabled on channel 0. 1 Legacy Voice enabled on channel 0.
2		UART_EN	This bit enables Legacy UART device. 0 UART disabled 1 UART enabled
1		JYSTK_EN	This bit enables Legacy Joystick device. 0 Joystick disabled 1 Joystick enabled
0		**ZVPORT**	**Enable ZVPORT, default 0 disable.**

Channel Format Register

Address **08**H

Bit(s)	R/W	Name	Description
31		CHB3D5C	Enable 5 channels sound at channel B.
30	FMOFFSET2	When Fmute=1, set this bit will initial FM PCM to offset 2 instead of ZERO, Default 0	
29		CHB3D	enable 4 channels sound at channel B.
28-24		VersionID	Read Only. “00”
23		SETLAT48	set Latency Timer 48\h
22		EDGEIRQ	when ‘1’, enable emulated edge trigger legacy IRQ to PCI bus #INTA, default 0
21		SPD24SEL	when ‘1’, and spd32sel=1 enable spdifout to play 24bit wave stream, default ‘0’
20-16		Reserved	
15-14		AdcBitLen[1:0] Sample resolution 00 16 Bits per sample . (Default) 01 15 Bits per sample. 10 14 Bits per sample. 11 13 Bits per sample.	
13-12		ADCDLEN	Sample method. ‘00” (default) Original mode ‘01’ Extra mode. ‘10’ 24k/22k mode. ‘11’ Weight mode.
11		CH1 Double sample rate from 48K to 96K.	
10		CH1 Double sample rate from 44.1K to 88.2K.	
9		CH0 Double sample rate from 48K to 96K.	
8		CH0 Double sample rate from 44.1K to 88.2K.	
7	INVSPDIFI	Invert XSPDIFI signal for reverse SPDIF stream format, Default ‘0’.	
6	DBLSPDS	Double SPDIF sampling rate to 96K, 88.2k when set this bit, Default ‘0’.	
5		POLVALID	Inverse SPDIF/IN Valid bit, default 0.
4		SPDLOCKED	A low active pulse to set read back status bit to ‘1’. When write ‘1’ to it will clear this bit to ‘0’.
3:2		CH1FMT[1:0]	Data format of channel 1 00 8 bit Mono mode 01 8 bit Stereo mode 10 16 bit Mono mode 11 16 bit Stereo mode
1:0		CH0FMT[1:0]	Data format of channel0 00 8 bit Mono mode 01 8 bit Stereo mode 10 16bit Mono mode 11 16 bit Stereo mode

Interrupt Hold/Clear Register

Address **0CH**

Bit(s)	R/W	Name	Description
31:24	R	VersionID	
		"08"	default
		"09"	PCB ID set.
		"0A"	Bound ID set.
		"0B"	Both PCBID and Bound ID set
23:19		Reserved	
18		TDMA_INT_EN	Interrupt hold/clear bits for updating TDMA position
		0	Interrupt Clear
		1	Interrupt Hold if exist.
17		CH1_INT_EN	Interrupt hold/clear bits for the Channel 1.
		0	Interrupt Clear
		1	Interrupt Hold if exist.
16		CH0_INT_EN	Interrupt hold/clear bits for the Channel 0.
		0	Interrupt Clear
		1	Interrupt Hold if exist.
15:0		Reserved	

Interrupt Register

Address **10**H

Bit(s)	R/W	Name	Description
31	R	INTR	Interrupt reflected from any sources. 0 No interrupt 1 Interrupt pending
30:28		Reserved	
27	R	VCO	
26	R	MCBint	Abort conditions occur during PCI Bus Target/Master Access. 0 No interrupt 0 Interrupt pending
25:17		Reserved	
16	R	UARTint	This bit is the UART interrupt bit. 0 No UART interrupt 1 UART interrupt pending
15:	R	LTDMAINT	Interrupt for updating Low Channel TDMA position. 0 No interrupt 1 Interrupt pending
14	R	HTDMAINT	Interrupt for updation High Channel TDMA position. 0 No interrupt. 1 Interrupt pending.
13:8		Reserved	
7	R	XDO46	Direct programming EEPROM interface , read data register
6	R	LHBTOG	High/Low status from DMA CTRL register.
5	R	LegHDMA	Legacy is in High DMA channel.
4	R	LegStereo	Legacy is in Stereo mode.
3	R	Ch1Busy	Channel B Busy.
2	R	Ch0Busy	Channel A Busy.
1	R	Chint1	Channel B Interrupt. 0 No interrupt 1 Interrupt pending
0	R	Chint0	Channel A Interrupt. 0 No interrupt 1 Interrupt pending

Legacy Control/Status Register

Address **14**H

Bit(s)	R/W	Name	Description
31		NXCHG	Don't map Base Register from Dword to Sample, default 0.
30:29		VMPU [1:0]	Base address for MPU401 access 00 Base address : 330h 01 Base address : 320h 10 Base address : 310h 11 Base address : 300h
28		ENWR8237	Enable Bus Master to Write 8237 Base Register, default 0.
27:26		VSBSEL[1:0]	The Base Address Select for SB16 access. 00 Base address: 220h 01 Base address: 240h 10 Base address: 260h 11 Base address: 280h
25:24		FMSEL[1:0]	The Base Address Select for FM access. 00 Base address : 388h 01 Base address : 3C8h 10 Base address : 3E0h 11 Base address : 3E8h
23		ENSPDOUT	enable XSPDIF/OUT to I/O Interface
22		SPDCOPYRHT	SPDIF IN/OUT CopyRight status bit
21		DAC2SPDO	enable Wave+FM+MIDI to SPDIF/OUT interface
20		INVIDWEN	Internal Vendor ID Write Enable when '1'. (default0)
19		C_EEACCESS	Direct programming EEPROM interface Registers.
18		C_EECS	
17		C_EEDI46	
16		C_EECK46	
15		CHB3D6C	Enable six-channel sound on Channel-B (CHB3D5C has to be set first)
14		CENTR2LIN	Line-in as center channel out
13		BASE2LIN	Line-in as bass channel out
12		EXBASEN	External bass input enable
11-0		Reserved	

Micellaneous Control Register

Address **18**H

Bit(s)	R/W	Name	Description
31		PWD	Power Down Mode enabled..
30		RESET	Reset Bus Master/DSP Engine.
29		Reserved	
28		VMGAIN	Additional analog master amp. +6dB gain control 0 Disabled, default setting 1 Enabled (boost +6dB gain, only valid if the master volume registers have been set with 0xFFh max. value.)
27		Reserved	
26		N4SPK3D	Hardware copy front channel to rear channel
25		SPDO5V	SPDIF-out level setting
24		W / SPDIF48K ; R / SPATUS48K ;	
23		ENDBDAC	Default low, High will enable Double DAC structure.
22		XCHGDAC	Default low, 0 CH0 > Front SPKR, CH1 > Back SPKR. 1 CH0 > Back SPKR, CH1 > Front SPKR.
21		SPD32SEL	when high, support 32bits SPDIF format ,low 16bits
20		SPDFLOOPI	internal SPDIF/OUT loopback to internal SPDIF/IN, for loopback testing
19		FM_EN	Legacy FM enabled.
18		AC3_EN	Enable AC3 control register in SPDIFOut format, default 0.
17		Reserved	
16		ENWRASID	Setting high choose to use the writable internal SUBID in the configuration space of the Audio function.
15		SPDF_AC97	0: SPDIF/OUT 44.1K 1:SPDIF/OUT 48K(share with AC97 transfer)
14		MASK_EN	Activate channel mask on Legacy DMA. 0 Disabled 1 Enabled
13		ENWRMSID	Setting high choose to use the writable internal SubID in the configuration space of the modem function.
12-9		Reserved	
8		SELSPDIFI2	Select secondary SPDIF In , default 0.
7		ENCENTER	Enable Center Channel, default 0.
6		MUTECH1	Mute PCI channel 1 to Analog DAC.
5		Reserved	
4		MIDSMP	Enable 1/2 interpolation at the Front end DAC..
3:2		UPDDMA[1:0]	For every the number of samples to notify updating TDMA position. 00 Every 2048 samples 01 Every 1024 samples 10 Every 512 samples. 11 Every 256 samples.
1		TWAIT1	The length of FM I/O cycle in unit of PCICLK. 0 48 PCICLKs. 1 64 PCICLKs.
0		TWAIT0	The length of I/O cycle but FM in unit of PCICLK. 0 4 PCICLKs. 1 6 PCICLKs.

T - DMA Position

Address **1C**H

Bit(s)	R/W	Name	Description
31:16	R	TDMACN T	Current Byte/Word Count of DMA channel.
15:0	R	TDMAADR	Current Address of DMA channel.

Mixer Control / Device Configure Register (can be accessed only by **BYTE** instruction)

Address **20**H

Bit(s)	R/W	Name	Description
7:0	W	SBVR[7:0]	Programmable SB16 version No.
	R	DEV[7:0]	Hardwire device version No.

Address **21**H

Bit(s)	R/W	Name	Description
7-3		Reserved	
2		X_ADPCM	SB16 ADPCM enable,default disabled.
1		PROINV	SBPro Left/Right channel switching.
0		X_SB16	Indicate device active as SB16 compatible, default SB16

Address **22**H

Bit(s)	R/W	Name	Description
7:0		IDXdata	Mapping SB compatible mixer INDEX register data port(A2x5h)

Address **23**H

Bit(s)	R/W	Name	Description
7:0		IDXaddr	Mapping SB compatible mixer INDEX register address port(A2x4h)

Address **24**H

Bit(s)	R/W	Name	Description
7		Fmmute	Mute FM
6		Wsmute	Mute Wave stream
5		REAR2LIN	Route REAR ch. Output to LINE-IN. default 0.
4		Rear2front	exchange rear and front channels's speaker out
3		Waveinl	Digital Wave recording Left channel
2		Waveinr	Digital Wave recording Right channel
1		X3DEN	3D surround enable.
0		Cdplay	SPDIF/IN PCM to DAC enable

Address **25**H

Bit(s)	R/W	Name	Description
7		RAUXREN	Recording source select R-Aux
6		RAUXLEN	Recording source select L_Aux
5		VAUXRM	R-AUX mute control
4		VAUXLM	L-AUX mute control
3:1		VADMIC[2:0]	Recording MIC volume control
0		MICGAINZ	MIC gain control,default high disable

Address **26**H

Bit(s)	R/W	Name	Description
7:4		VAUXL[3:0]	L-AUX volume control
3:0		VAUXR[3:0]	R-AUX volume control

Address **27**H

Bit(s)	R/W	Name	Description
0		DMAUTO	SB16 Low/High DMA Auto detect enabled ,When high.
1		SPDVALID	SPDIF/IN valid bit detect enabled, When high.
2		XGPBIO	general purpose bi-direction pin, when high output tri-state (default LOW)
3		Reserved	
4		Reserved	
5		XGPO1	general purpose output pin 1,this pin shared with XSPDIFO pin, and enabled when index reg. F0_bit 0 programmed high.
6:7		Reserved	

* In test mode Reg. 27H is used to testing analog ADC testing.

MPU401 PCI Port

Index address **40-4F**H

FM PCI Port

Index address **50-5F**H

Extension Index Register (access from SB compatible mixer port)

Index address **F0**H

Bit(s)	R/W	Name	Description
7:5		VPHONE[2:0]	Phone volume control
4		VPHOM	Phone mute control
3		VSPKM	PC-Speaker mute control, default high un-mute
2		RLOOPREN	Recording R-channel enable
1		RLOOPLEN	Recording L-channel enable
0		VADMIC3	Microphone record boost, default low disable, high enable.

Analog Testing Register

Address **70-71**H

Bit(s)	R/W	Name	Description
15:0		ANATAT[15:0]	The settings of analog test mode (Reserved)

Channel 0 Frame Register 1

Address **80**H

Bit(s)	R/W	Name	Description
31:0	W	BASADDR0	Base address of channel 0.
	R	CURADDR0	Current address of channel 0.

Channel 0 Frame Register 2

Address **84**H

Bit(s)	R/W	Name	Description
31:16	W	BASCNT0	Base count of samples at Codec.
15:0	W	BASCNT0	Base count of samples at Bus Master.
31:16	R	CURCNT0	Current count of samples at Codec.
15:0	R	CURCNT0	Current count of samples at Bus Master.

Channel 1 Frame Register 1

Address **88**H

Bit(s)	R/W	Name	Description
31:0	W	BASADDR1	Base address of channel 0.
	R	CURADDR1	Current address of channel 0.

Channel 1 Frame Register 2

Address **8C**H

Bit(s)	R/W	Name	Description
31:16	W	BASCNT1	Base count of samples at Codec.
15:0	W	BASCNT1	Base count of samples at Bus Master.
31:16	R	CURCNT1	Current count of samples at Codec.
15:0	R	CURCNT1	Current count of samples at Bus Master.

Miscellaneous Control Register

Address **92-3**H

Bit(s)	R/W	Name	Description
15:13		Reserved	
12	W/R	**ADC48K44K**	
		'0' (default)	ADC uses parameters for 44k group.
		'1'	ADC uses parameters for 48k group.
11:5		Reserved	
4	W/R	**SPD32KFMT**	
		'0' (default)	SPDIF/IN uses 44/48k sampling rate.
		'1'	SPDIF/IN uses 32k sampling rate.
3	W/R	**ADC2SPDIF**	
		'0' (default)	ADC output is not connected to SPDIF/OUT.
		'1'	ADC output is connected to SPDIF/OUT.
2	W/R	**SHAREADC**	
		'0' (default)	The DAC part inside ADC block is not shared out.
		'1'	The DAC part inside ADC block is shared out.
1	W/R	**REALTCMP**	
		'0' (default)	Pin XGD6,XGD7 are for game port use.
		'1'	Pin XGD6, XGD7 are used to monitor CMPL/CMPR of the ADC.
0	W/R	**INVLRCK**	Setting high inverts ZVPORT's signal LRCK.
		'0' (default)	Pin LRCK for ZVPORT is not inverted.
		'1'	Pin LRCK for ZVPORT is inverted.

Legacy SB compatible mixer

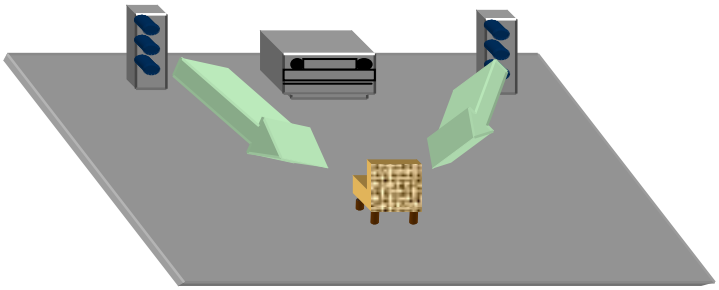
Index	D7	D6	D5	D4	D3	D2	D1	D0
0x00	Reserved							
0x04	Wave volume left channel				Wave volume right channel			
0x0A						Mic volume		
0x22	Master volume left channel				Master volume right channel			
0x26	FM volume left channel				FM volume right channel			
0x28	Analog-CD volume left channel				Analog-CD volume right channel			
0x2E	Line-In volume left channel				Line-In volume right channel			
0x30	Master Volume L.							
0x31	Master Volume R.							
0x32	Wave volume L.							
0x33	Wave volume R.							
0x34	MIDI Volume L.							
0x35	MIDI Volume R.							
0x36	CD Volume L.							
0x37	CD Volume R.							
0x38	Line-In Volume L.							
0x39	Line-In Volume R.							
0x3A	Mic. Volume							
0x3B	PC spk volume							
0x3C				Output muting controls				
				Line L	Line R	CD L	CD R	Mic
0x3D		Recording left channel controls						
		FM L	FM R	Line L	Line R	CD L	CD R	Mic
0x3E		Recording right channel controls						
		FM L	FM R	Line L	Line R	CD L	CD R	Mic
0x3F	Reserved							
0x40	Reserved							
0x41	Reserved							
0x42	Reserved							
0x43	Reserved							
0x44	Reserved							
0x45	Reserved							
0x46	Reserved							
0x47	Reserved							

Please do not write any values into reserved registers
0x30-0x3A registers are SB16 compatible and will be linked with 0x04-0x21 SB Pro registers correspondingly.
Only 0x30-31 master volume registers are 5 bits and the other are 4 bits.

9. Audio Processing Technology

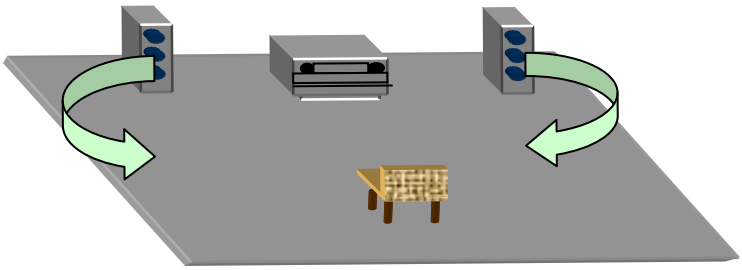
9.1 Stereo

It is only one-dimensional, as sounds come from (left /right) the physical location of speakers.



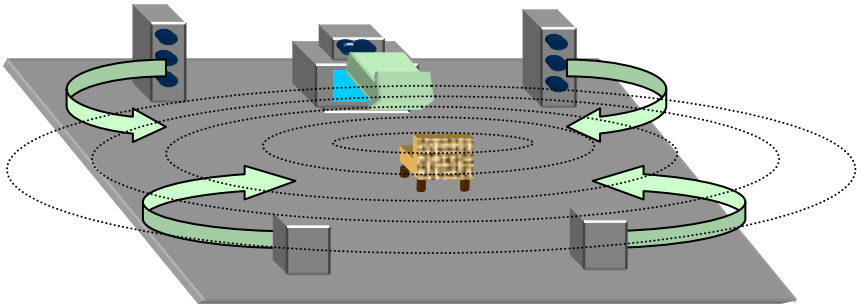
9.2 Surround (Stereo Expander)

It filters the existing stereo signal to make the sounds fill in the area around the speakers, and in front of the listener. Sound sources appear to come from outside the physical locations of the speakers.



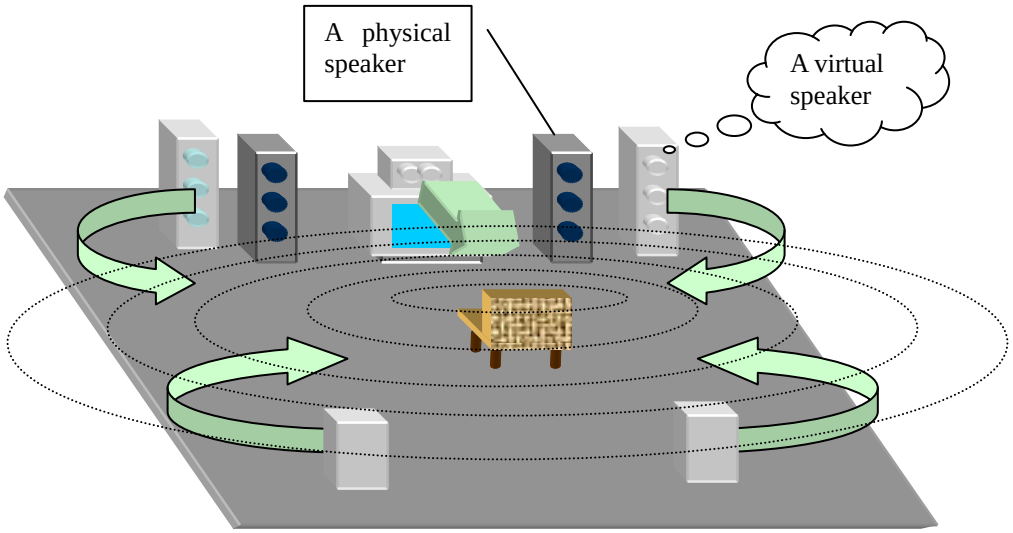
9.3 Multi-Speaker Surround (Dolby Pro Logic or Digital AC-3)

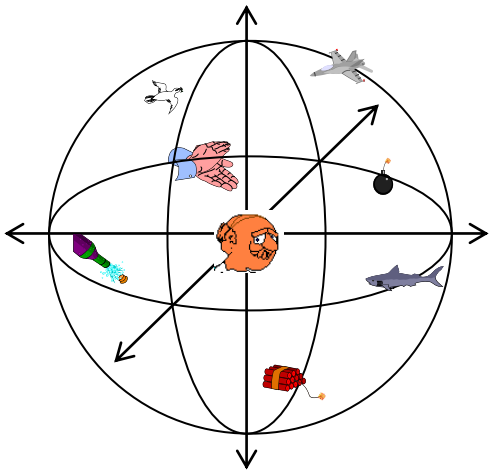
It uses five speakers instead of two to surround the listener; hence, sound sources come from five directions and create engaging audio experience. This surround sound effect, however, has to be pre-recorded, and it dose not support interactive environment.



9.4 HRTF 3D Positional 3D (C-Media 3D)

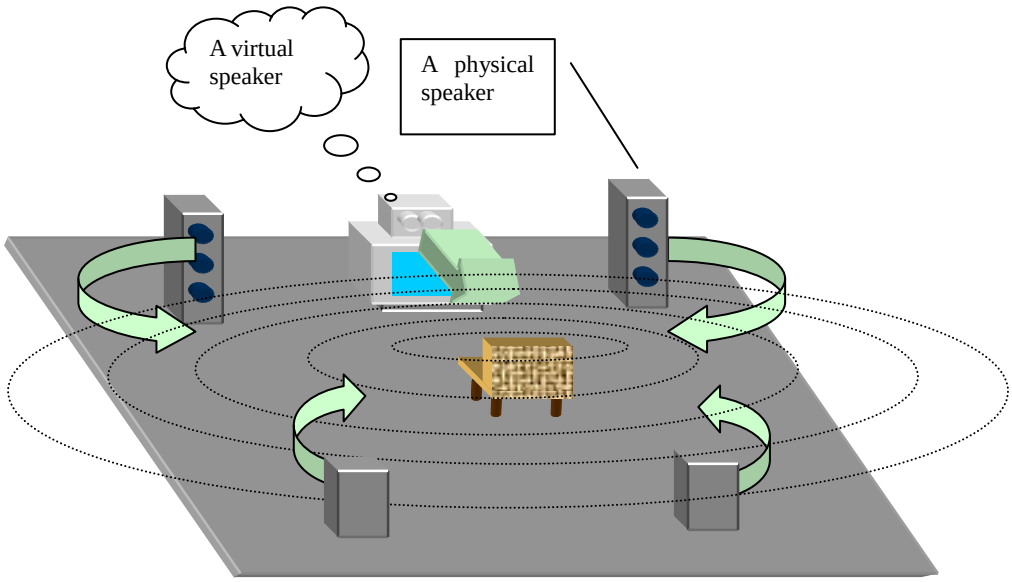
Only this sound processing technology can be called real 3D manifestation, as 3D usually refers to the three dimensions of X, Y and Z. This technology allows people to pin-point the location of sound in the real world (up/down, left/right, front/back)using only two speakers or a pair of headphones. This technology also supports interactive 3D applications to get a real-time placement of sounds via API (application programming interface) such as Microsoft DirectSound3DTM. We can also use this technology to simulate Multi-speaker Surround with two physical speakers to deliver five “virtual" speakers in the air, surrounding the listener and creating home theater sound environment. This is the most economical and the easiest solution to people who would like to get high performance surround sound but don’t want to spend money in adding extra speakers.





9.5 HRTF 3D Extension Positional (C-Media 3DX)

3D illusion exists because traditional 3D positional audio system assumes the user's position as the sweet spot to design crosstalk-cancellation circuit; therefore, if the user wants to have 3D positional audio effects, he can't move his head or position out of sweet spot. Another 3D illusion fails because half the population are compulsive "head-turners" who will never get 3D audio from two speakers . To remedy this, C-Media utilizes HRTF 3D extension technology (C3DX) to enhance traditional HRTF 3D positional audio by substituting two-speaker system by four-speaker one. Therefore, at least one or two speakers should be placed behind the listener's head to complement the rear-side effect, thus creating compelling realistic sound. This technology greatly improves HRTF 3D positional audio quality, and successfully eliminates the sweet spot limitation. Users can enjoy the real 3D audio gaming effects, and don't have to worry about the environmental confinement any more.



9.6 C3D Positional Audio Technology White-Paper

C3D Positional Audio Technology White-Paper

C3D HRTF Positional Audio Technology

The basic concept of C3D is: since we can hear sound three dimensionally in the real world using our two ears, it must be possible to regenerate the same sound effect from two loud speakers.

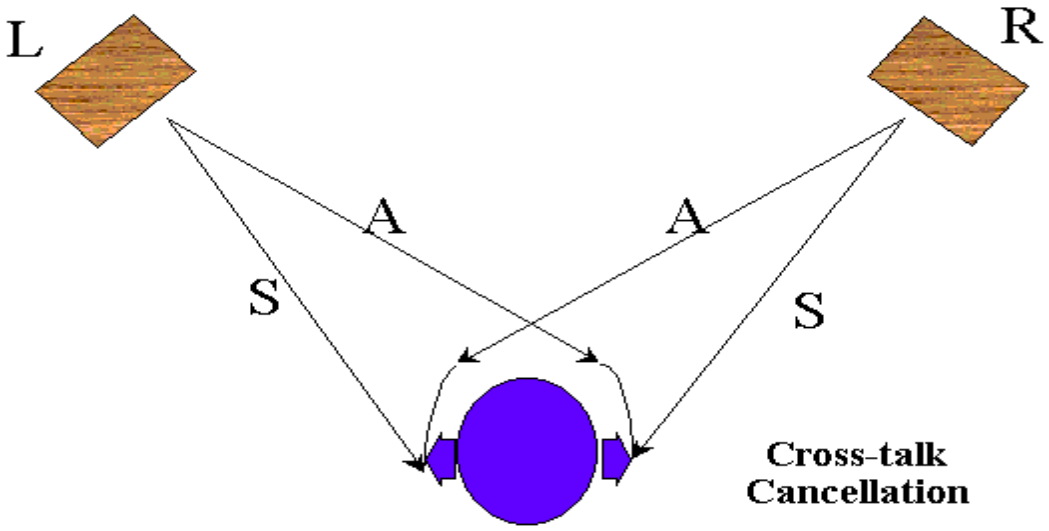
How to listen to C3D sound correctly and properly?

a. Use Headphones to Have Much Better Effect

When you use headphones in listening, there will be less interference such as outside voices or room reflections comparing to using speakers.

b. Choose Correct Output Devices

Choose the correct output devices in the options of demo program in accordance with what listening devices you want to listen to. Listening through speakers must be proceeded by crosstalk-cancellation, so if you choose the wrong output devices, there won't be any 3D positional audio effect.

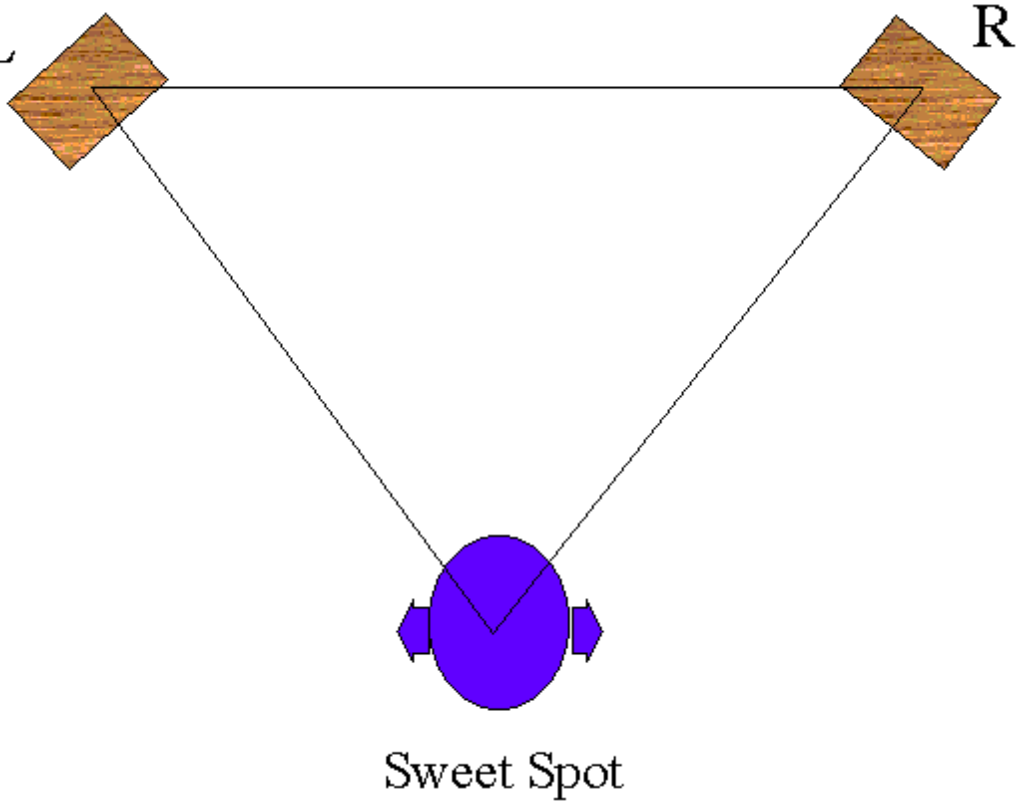


c. Position of Speakers

If you listen from speakers, please do not reverse the left and right speakers, which should be put in equal distance from the listener. That is, the listener, the left, and the right speaker must be in the topmost of a right triangle. The position of the listener is called the “sweet spot”. In addition, the height of the listener’s ears must be equal to that of the speakers.

9.7 Turn Surround Sound Functions off

When the surround sound effect is enabled, it will cause confusion with C3D sound, and make positional sound effect invalid.



10. CMI8738 PCI Audio Adapter Layout Notes

1. The wires of analog circuits(chip pin64-80) must be wider than 12mil.
2. Placing digital signals such as SPDIF IN/OUT(pin86, 98) and TXD/RXD(pin88,89) near the analog signals should be avoided. However, if these signals have to be adjacent, please place ground between these digital and analog signal wires to isolate noises.
3. The whole PCB grounding should be well-organized(The ground must be placed as much as possible. Also, the ground of both the component and the solder sides should be drilled as much as possible.).
4. The grounding under CMI8738 should be well-organized as mentioned above.
5. The regulator(78L05) must be placed near the chip as much as possible.
6. The chip and the circuits need independent power supply regulators to prevent insufficient currents.

Revision Release Note:

V1.7 12/17/2001
Add register listing.

V1.8 12/31/2001
Modify chip digital power pins level range.

V1.8c 02/18/2002
Pin description list arrangement.

V1.8d 07/09/2003
Corrected register 24h bit5 (REAR2LIN) and register 18h bit5 (Reserved).

— End of Specifications —

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